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EXAMINER	
PHAM, TAMMY T	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,912	KIM ET AL.	
	Examiner	Art Unit	
	Tammy Pham	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-12,14-32 and 34-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-12,14-32 and 34-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Claims 4, 13, 33 have been cancelled. Claims 1-3, 5-12, 14-32, 34-47 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-3, 5-8 and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cairns et al. (US Patent Application: 2002/0030652 A1) {from here on referred to as Cairns1} in view of Cairnes et al. (US Patent No: 6,268,841 B1) {from here on referred to as Cairns2}.

As for claim 1, Cairns1 teaches of a data driving apparatus (2) for a liquid crystal display device (Fig. 1), comprising:

a first multiplexer (13) part performing a time-division on inputted digital pixel data;

a digital-analog converter (12) part converting the time-divided digital pixel data from the first multiplexer (13) part to analog pixel signals;

a demultiplexer (14) part supplying the analog pixel signals from the digital-analog converter (12) part to a plurality of output channels in section [0015] and in Fig. 4;

Cairns1 fails to teach of an output sampling part.

Cairns2 teaches of an output part sampling and holding first received analog pixel signals from the demultiplexer (14) part and holding second received analog pixel signals and simultaneously outputting both first and second received pixel signals to corresponding data lines.

wherein the output part comprises:

a sampling part (25) sampling the pixel signals from odd-numbered or even-numbered output channels of the demultiplexer (14) part;

a capacitor part (52) receiving and holding the sampled pixel signals from the output channels of the demultiplexer (14) part;

an output buffer (40) part coupled to the capacitor part (52) in Fig. 12 and in column 10, lines 18-41.

It would have been obvious to one with ordinary skill in the art at the time the invention was made to combine the output part of Cairns2 with the rest of the components of the data driving apparatus of Cairns1 in order to have fewer converters (see Cairns2: column 4, line 34).

Neither Cairnes1 nor Cairnes2 teaches of a third multiplexer part.

Examiner takes official notice that it would be obvious for one to include a third multiplexer part simultaneously discharging the pixel signals held in the capacitors to the corresponding data lines through the output buffer (40) part in order to better control the various signal lines coming in. For further reference, please refer to US Patent No: 5361081, 5892493, 6333729, 6734865, 6847346 which shows that it is common in the art to have a multiplexer output to the data lines.

It would have been obvious to one with ordinary skill in the art at the time the invention was made to include a third multiplexer with the existing combination of Cairns1 and Cairns2 so that one can control the various lines of data coming out of the data driver.

As for claim 2, Cairns1 teaches that the apparatus according to claim 1, wherein the digital-analog converter (12) part coupled to the output channels of the demultiplexer (14) part in Fig. 4 and in section [0015].

As for claim 5, Cairns1 teaches of

a shift register (10) sequentially shifting an input source start pulse in accordance with an input source shift clock to generate a sampling signal; and

a latch part (11) sequentially latching the pixel data in response to the sampling signal and simultaneously providing the latched pixel data to the first multiplexer (13) during an enable period of an input source output enable signal in Fig. 4 and in section [0015].

As for claim 6, the combination of Cairns1 and official notice (as stated in claim 1 above) teaches of the second multiplexer provides the corresponding data lines with the pixel signals held in the capacitors for the enable period of the source output enable signal and a reference voltage of liquid crystal cells for the disabled period of the source output enable signal in section [0051].

As for claim 7, Cairns1 teaches that the first multiplexer (13) and the demultiplexer (14) part are controlled by an ODD/EVEN signal which performs the time-division for a horizontal period in section [0051].

As for claim 8, Cairns2 teaches that the sampling switches controlled by an ODD/EVEN signal which performs the time-division on a horizontal period in column 1, lines 54-58.

As for claim 30, Cairnes1 teaches that a data driving method for a liquid crystal display device (Fig. 1), comprising:

performing a time-division on a digital pixel data;

converting the time-divided digital pixel data into time-divided analog pixel signals;

supplying the time-divided analog pixel signals to corresponding output channels in Fig. 4 and in section [0015];

Cairnes1 fails to teach of a sampling and holding section.

Cairnes2 teaches of sampling and holding first inputted pixel signals through a first part of the output channels and holding second inputted pixel signals from a second part of the output channels, and simultaneously supplying the first and second held pixel signals corresponding data lines and

buffering the held pixel signals through an output buffer (40) part prior to supplying the held pixel signals to the corresponding data lines, wherein the output buffer (40) part is connected to the corresponding data lines in Fig. 12 and in column 10-41.

It would have been obvious to one with ordinary skill in the art at the time the invention was made to combine the output part of Cairns2 with the rest of the components of the data driving apparatus of Cairns1 in order to have fewer converters (see Cairns2: column 4, line 34).

As for claim 31, Cairns2 teaches that the method according to claim 30, wherein the first and second held pixel signals are supplied to the corresponding data lines for an enable period of an input source output enable signal and a reference voltage of liquid crystal cells is commonly supplied to the corresponding data lines for a disable period in Fig 12.

2. Claims 9-12, 14-29, 32, 34-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cairns et al. (US Patent Application: 2002/0030652 A1) {from here on referred to as Cairns1} in view of Cairnes et al. (US Patent No: 6,268,841 B1) {from here on referred to as Cairns2} and Nitta et al. (US Patent No: 6,661,402 B1).

As for claim 9, Cairns1 teaches of a data driving apparatus (2) for a liquid crystal display device (Fig. 1), comprising:

a multiplexer part performing a time-division on inputted digital pixel data and providing the time-divided pixel data through output channels;

a digital-analog converter (12) part converting the time-divided digital pixel data from the multiplexer into analog pixel signals;

a demultiplexer (14) part providing the time-divided pixel signal from the digital-analog converter (12) to different output channels in Fig. 4 and in section [0015];

Cairns1 fails to teach of an output sampling part or of a discharging part discharging the pixel signals held in the holding part for a first period.

Cairns2 teaches of an output part sampling and holding the time-divided pixel signals from the demultiplexer through a path and outputting the pixel signals to corresponding data lines for a next horizontal period

wherein the output part comprises:

a sampling part (25) sampling the pixel signal supplied through the output channels of the demultiplexer (14) and providing the sampled pixel signal to corresponding paths;

a holding part holding the pixel signals provided through the corresponding paths of the sampling part (25) in Fig. 12 and in column 10, lines 18-41. As for the discharging part discharging the pixel signals held in the holding part for a first period, the purpose of storage capacitors control the light of each pixel by charging and discharging.

It would have been obvious to one with ordinary skill in the art at the time the invention was made to combine the output part of Cairns2 with the rest of the components of the data driving apparatus of Cairns1 in order to have fewer converters (see Cairns2: column 4, line 34).

Cairns1 and Cairns2 fails to teach of the components of the driving apparatus having selected polarity.

Nitta teaches of the components of the driving apparatus having selected polarity via positive and negative output channels/paths in column 3, lines 23-33 and in column 4, lines 25-30.

It would have been obvious to one with ordinary skill in the art at the time the invention was made to have selected polarity as taught by Nitta with the various components of the driving apparatus of taught by Cairn1 in order to increase the speed and functionality of the driver (see Nitta: column 1, lines 50-55).

As for claim 10, the combination of Cairns1 and Nitta teaches that the digital-analog converter (Cairns1: 12) part comprises:

a positive digital-analog converter (Cairns1: 12) converting the pixel signals provided through positive output channels of the multiplexer into positive pixel signals; and

a negative digital-analog converter (Cairns1: 12) converting the pixel signals provided through negative output channels of the multiplexer into negative pixel signals in Fig.4 and section [Cairns1: 0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 11, the combination of Cairns1 and Nitta teaches that the multiplexer part comprises:

a plurality of positive path switches coupled to input channels for the pixel data and commonly connected to positive output channels; and

a plurality of negative path switches coupled to the input channels for the pixel data in parallel, connected to the positive path switches in parallel, and commonly connected to negative output channel in Fig.4 and section [0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 12, the combination of Cairns1 and Nitta teaches that the demultiplexer (14) part comprises:

a plurality of positive path switches forming a plurality of different positive paths, and commonly connected to a positive digital-analog converter, wherein the positive path switches connected to output channels of the positive digital-analog converter (12); and

a plurality of negative path switches forming a plurality of different negative paths, commonly connected to a negative digital-analog converter (12), wherein the negative path switches are connected to the positive path switches in parallel and connected to the positive channel switches of the output channels of the negative digital-analog converter in Fig.4 and section [0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 14, Cairns2 teaches that the sampling part (25) and the holding part sample and hold the pixel signals supplied for the second period through the channel different from that of the pixel signal supplied for the first period in Fig. 12. One can see that each column has at least three sets of buffers.

As for claim 15, the combination of Cairns2 and Nitta teaches that the sampling part (25) has a second demultiplexer (14) part comprising;

a plurality of the positive path switches forming a plurality of different positive paths and connected to the output channels of the demultiplexer (14) part; and

a plurality of negative path switches connected to the output channels of the demultiplexer (14), and connected to the positive path switches in parallel in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 16, the combination of Cairns2 and Nitta teaches that the holding part comprises:

a positive path capacitor charging and holding the positive pixel signals from the positive path switches of the second demultiplexer (14) part; and

a negative path capacitor charging and holding the negative pixel signals from the negative path switches of the second demultiplexer (14) part in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 18, the combination of Cairns2 and Nitta teaches that the multiplexer, the demultiplexer (14), and the second demultiplexer (14) are controlled by a first control signal through an input polarity control signal and an ODD/EVEN signal performing the time-division on a horizontal period in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 19, the combination of Cairns2 and Nitta teaches that the ODD/EVEN signal performsthe time-division on an enable period determined by a source output enable signal for the horizontal period in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 20, the combination of Cairns2 and Nitta teaches that the ODD/EVEN signal further performs the time-division on a disable period of the source output enable signal in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 21, the combinations of Cairnes1 and Nitta teaches that the multiplexer part, the demultiplexer (14) part in Fig.4 and section [0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}. The combination of Cairns2 and Nitta teaches that the second demultiplexer (64) part recharge the holding part with the pixel signals for the disable period, wherein the pixel signals are generated for a previous enable period in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 22, the combinations of Cairnes2 and Nitta teaches that the source output enable signal is generated by increasing the disable period of an external reference source output enable signal in order to secure a recharging period of the holding part in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 23, the combinations of Cairnes2 and Nitta teaches the second multiplexer part is controlled by the first control signal and a second control signal that is phase-inversed

with respect to the first control signal in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 24, the combinations of Cairnes2 and Nitta teaches that an output buffer (40) part buffering the pixel signal discharged from the holding part to the discharging part in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 25, the combinations of Cairnes2 and Nitta teaches that the output buffer (40) part comprises:

a plurality of positive path output buffer (40)s connected between the positive path capacitors of the holding part and the positive path switches of the second multiplexer part; and

a plurality of negative path output buffer (40)s connected between the negative path capacitors of the holding part and the negative path switches of the second multiplexer part in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 26, the combinations of Cairnes2 and Nitta teaches that the output buffer (40) part buffering the pixel signal supplied through the output channels of the second multiplexer part and supplying the pixel signals to each of the data lines in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 27, the combinations of Cairnes2 and Nitta teaches that the output buffer (40) part comprises: a plurality of output buffer (40)s connected between the output channels of the second multiplexer part and the data lines in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 28, the combinations of Cairnes1 and Nitta teaches of:

a shift register (10) sequentially shifting an input source start pulse in accordance with an input source shift clock to generate a sampling signal;

a latch part (11) latching pixel data and simultaneously providing the multiplexer part with the latched pixel data for the enable period of the input source output enable signal; and

a level shifter part raising a voltage of the pixel data from the multiplexer part to supply the pixel data to the digital-analog convert part in Fig.4 and section [0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 29, the combinations of Cairnes2 and Nitta teaches that a third multiplexer part supplying the pixel signals from the output part to the corresponding data lines for the enable period of the source output enable signal and commonly supplying a reference voltage of the liquid crystal cells to the corresponding data lines for the disable period of the source output enable signal in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 32, the combinations of Cairnes1 and Nitta teaches that the time-divided digital pixel data comprises:

converting the time-divided pixel data to a positive analog pixel signal and a negative analog pixel signal; and

selecting one of the positive and the negative analog pixel signals in accordance with a polarity control signal in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 34, the combinations of Cairnes2 and Nitta teaches that the sampling the pixel signals is controlled by an ODD/EVEN signal performing a time-division on a horizontal period in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 35, Cairnes1 teaches that a data driving method for a liquid crystal display device (Fig. 1).

Performing a time-division on a digital pixel data and providing the time-divided digital pixel data through output channels;

converting the time-divided digital pixel data into analog pixel signals in Fig. 4 and in section [0015].

Cairnes1 fails to teach of a sampling and holding the time-divided analog pixels.

Carines2 teaches of sampling and holding the time-divided analog pixel signals to output channels;

outputting the held pixel signals to corresponding data lines for a next horizontal period in Fig. 12 and in column 10, lines 18-41.

It would have been obvious to one with ordinary skill in the art at the time the invention was made to combine the output part of Cairns2 with the rest of the components of the data driving apparatus of Cairns1 in order to have fewer converters (see Cairns2: column 4, line 34).

Cairns1 and Cairns2 fails to teach of the components of the driving apparatus having selected polarity.

Nitta teaches of the components of the driving apparatus having selected polarity using positive and negative channels and paths in column 3, lines 23-33 and in column 4, lines 25-30.

It would have been obvious to one with ordinary skill in the art at the time the invention was made to have selected polarity as taught by Nitta with the various components of the driving apparatus of taught by Cairns1 and Carins2 in order to increase the speed and functionality of the driver (see Nitta: column 1, line 28).

As for claim 36, the combination of Cairns1 and Nitta teaches that the performing a time-division on a digital pixel data and the converting the time-divided digital pixel data are controlled by an input polarity control signal and a first control signal through an ODD/EVEN signal performing a time-division on a horizontal period in Fig. 4 and in section [0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 37, the combination of Cairns1 and Nitta teaches that the ODD/EVEN signal performs a time-division on an enable period determined by a source output enable signal in Fig. 4 and in section [0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 38, the combination of Cairns1 and Nitta teaches that the ODD/EVEN signal performs a time-division on a disable signal of a source output enable signal in Fig. 4 and in section [0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 39, the combination of Cairns1 and Nitta teaches the pixel signals are sampled and held by the ODD/EVEN signal for the disable period, wherein the pixel signals in a present enable period are the same as the pixel signals in a previous enable period in Fig. 4 and in section [0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 40, the combination of Cairns1 and Nitta teaches the disable period of the source output enable signal is determined by increasing the disable period of a reference source output enable signal inputted from an external source in Fig. 4 and in section [0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 41, the combination of Cairns1 and Nitta teaches that the outputting the held pixel signals is controlled by a first control signal and a second control signal having a phase inversion with respect to the first signal in Fig. 4 and in section [0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 42, the combination of Cairns1 and Nitta teaches the performing a time-division on a digital pixel data is carried out by outputting the time-divided pixel data with a polarity through the time-divided pixel data of the output channel opposite to that of the time-divided pixel data for a previous period and an adjacent channel in Fig. 4 and in section [0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 43, the combination of Cairns1 and Nitta teaches that the performing a time-division on a digital pixel data is carried out by converting the time-divided pixel data into the time-divided pixel data with a polarity opposite to that of the time-divided analog signal of a previous period and an adjacent channel in Fig. 4 and in section [0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 44, the combination of Cairns2 and Nitta teaches that the sampling and holding the time-divided analog pixel signals is performed by sampling and holding the time-divided pixel signal through a path with a polarity opposite to that of time-divided pixel signal of a previous period and an adjacent channel in Fig. 12 and in column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 45, the combination of Cairns2 and Nitta teaches the output held pixel signals is buffered through an output buffer (40) part prior to supplying to the corresponding data lines, wherein the output buffer (40) part is connected to the corresponding data lines in Fig. 12 and in column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 46, the combination of Cairns1 and Nitta teaches that the held pixel signals are supplied to the corresponding data lines for the enable period of an input source output enable signal, and a reference voltage of the liquid crystal cells is commonly supplied to the corresponding data lines for the disable period in Fig. 4 and in section [0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 47, the combination of Cairns2 and Nitta teaches of raising a voltage of the time-divided pixel data after the performing a time-division on a digital pixel data in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 3, the combination of Cairns1 and Nitta teaches that the digital-analog converter (12) part comprises:

a positive digital-analog converter (12) converting the digital pixel data to a positive pixel signal;

a negative digital-analog converter (12) converting the digital pixel data to a negative pixel signal (see Nitta: column 3, line 26); and

a second multiplexer part selecting one of the positive and the negative pixel signals in accordance with a polarity control signal and providing the selected pixel signal with the demultiplexer (14) part in Fig.4 and section [0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

As for claim 17, the combination of Cairns2 and Nitta teaches that the discharging part comprises:

a plurality of positive path switches connected to the positive path switches of the second demultiplexer (14) through the holding part and connected to the data lines; and

a second demultiplexer (14) part having the negative path switches connected to the negative switches of the second demultiplexer (14) through the holding part and connected to the negative channel switches and the data lines in parallel in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

Response to Arguments

Applicant's arguments filed 6/21/2006 have been fully considered but they are not persuasive.

In regards to the argument of claim 1 on page 13, paragraph 2 of the applicant's remarks, specifically that there the previous non-final rejection lacked requisite documentary to show that the third multiplexer that correspond to the data line, please refer to US Patent No: 5361081,

5892493, 6333729, 6734865, 6847346 which shows that it is common in the art to have a multiplexer output to the data lines.

In regards to the argument of claim 9 on page 15, paragraph 2 of the applicant's remarks, specifically that neither of the references teach that "a discharging part discharging the pixel signals held in the holding part for a first period to the corresponding data line through the different polarity paths for a second period," please refer to Nitta in column 3, lines 23-33 and in column 4, lines 25-30 for teaching of the corresponding data line through the different polarity paths for a second period. Also keep in mind that Cairns2 teaches of storage capacitors which control the lighting of each pixel by charging and discharging.

In regards to the argument of claim 35 on page 17, paragraph 1 of the applicant's remarks, specifically that "an increase the speed and functionality of the driver is not attributable to the components of the driving apparatus having selected polarity, but to other features as described in the quoted portion of Nitta," please refer to Nitta, column 8, line 28 where Nitta states that by applying a separate voltage for positive and negative polarity write time, this process allows data to be written into the LC panel at a high speed.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tammy Pham whose telephone number is (571) 272-7773. The examiner can normally be reached on 8:00-5:30 (Mon-Fri).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tammy Pham
August 25, 2006

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